REMARKS

The undersigned appreciates the indication that Claims 1-11, 13, 25-29, 31-39 and 41-46 have been allowed.

Claims 14-22, 47 and 48 are rejected under 35 U.S.C. 103a as being unpatentable over U.S. Patent 6,262,704 to *Kurumisawa et al.* in view of U.S. Patent 5,764,225 to *Koshobu*. The rejection is respectfully traversed.

The Examiner is of the opinion that "*Kurumisawa* teaches how at least one of the electrical potentials supplied to the display matrix floats with a voltage supplied by electrically isolating the matrix", referring to Column 20, Lines 55-63 and Column 21, Lines 21-28 and Figures 34A and 34B of *Kurumisawa*. We respectfully disagree.

As noted by *Kurumisawa*, in Column 21, Lines 16-20, at least one of the switches 711, 726 is open during a high-impedance mode. The current path is, therefore, disconnected and unnecessary current never flows. This reduces power consumption. Since at least one of the switches 711, 726 is open, whatever voltage that may be present on the scanning lines or the data lines connected to the switches cannot change with any other voltage or voltage range. *Kurumisawa*, in Column 21, Lines 29-34, continues: "In the liquid-crystal panel shown in FIG. 34A, switches 711.about.716 within switch means 710 and switches 721.about.726 within switch means 720 are all opened. Therefore, the scanning lines L1.about.L6 and the data lines S1.about.S6 are all set to an electrically floating state." In other words, the current paths through these switches and therefore through all of the scanning lines and the data lines connected to the switches in the liquid-crystal panel shown in FIG. 34A are disconnected from any power source or voltage and unnecessary current never flows through them, so that the voltages on these lines cannot change with any other voltage or voltage range. Therefore, contrary to the opinion of the Examiner, the so-called "electrical potentials supplied to the display matrix" in *Kurumisawa* do not float with any other voltage, since no electrical potentials are supplied to the display matrix in the first place in the sections of *Kurumisawa* relied on by the examiner in the rejection.

In claim 14 one or more of the power sources drives the row electrodes through a first voltage range, and drives row column electrodes through a second voltage range. Claim 14 has been amended in that the first voltage range changes so that it has two

distinct and different ranges of values over different field addressing cycles. As pointed out by the undersigned during the interview with the examiner on May 5, 2004, in one embodiment, the first voltage range that the row electrodes are driven in claim 14 is illustrated by the range V1 to V5 in the field 2xN in Fig. 2a. During the field 2xN+1, the first voltage range is V2 to V6. In such embodiment, during the field 2xN, the second voltage range is from V4 to V6 and during the field 2xN+1, the second voltage range is between V1 and V3. *Koshobu* employs two separate power sources 70 and 80 for driving the row (scanning) and column (signal) electrodes respectively. As described by *Koshobu* in column 6, line 59 through column 7, line 32, Ve is generated by the circuit 40 in Fig. 7 from VEE1 and VSS1 from source 70. The eight drive voltages V1-V8 for driving the column or signal electrodes are generated by the circuit 50 in Fig. 8 from VEE2 and VSS2 from source 80, with Ve from circuit 40 as a reference. In this manner, "even where the output voltages VEE1, VSS1, VEE2 and VSS2 of the power supply circuits 70 and 80 fluctuate for example, the power supply voltages to the scanning electrode drive circuit 20 and the signal electrode drive circuit 30 do not fluctuate relative to each other and a direct current voltage component can be prevented from being applied to the liquid crystals." Column 7, lines 21-32. In other words, when voltages VEE1, VSS1, VEE2 and VSS2 of the power supply circuits 70 and 80 fluctuate, there may be fluctuations in the voltages applied by circuits 40 and 50 to the row (scanning) and column (signal) electrodes. By causing V1-V8 to be generated using Ve as a reference, V1-V8 will not fluctuate relative to the output voltages Vwp, Vhp, Ve, Vhn and Vwn of circuit 40 despite fluctuations in VEE1, VSS1, VEE2 and VSS2. In reference to the above-referenced characteristics of the first voltage range of claim 14, however, *Koshobu* fails to disclose that the output voltages Vwp, Vhp, Ve, Vhn and Vwn of circuit 40 for driving the row (scanning) electrodes have two distinct and different ranges of values over different field addressing cycles. Instead, these fluctuations would appear to follow those of VEE1, VSS1, VEE2 and VSS2 of the two power supplies, and may be random in nature. *Kurumisawa* likewise fails to disclose the above-referenced characteristics of the first voltage range of claim 14,

Thus, *Kurumisawa* and *Koshobu* both fail to teach or suggest the above-described feature of Claim 14 (the first voltage range changes so that it has two distinct and

different ranges of values over different field addressing cycles) so that the combination of *Koshobu* and *Kurumisawa* also fails to teach or suggest claim 14. Claim 14 is, therefore, believed to be allowable.

The examiner admits that *Kurumisawa* fails to teach two separate power sources, but is of the opinion that this missing teaching is supplied by *Koshobu*. However, there appears to be no reason or motivation to combine *Koshobu* and *Kurumisawa*. The reason given by the examiner for the combination (to provide a display capable of easily reducing flicker) simply does not apply to *Kurumisawa*. As noted above, *Kurumisawa*. is primarily interested in reducing power use, and in fact is turning off a portion or all of the display to reduce power consumption, and not to reduce flicker. There is therefore no reason or motivation to combine *Koshobu* and *Kurumisawa,* and the rejection also fails for this reason.

The examiner rejects claims 15-22 and 47 on the ground that they depend on a rejected independent claim. This is not a valid ground for rejecting claims.

Claims 15-22 are believed to be allowable since they depend from allowable Claim 14. They are further believed to be allowable on account of the features in these claims. The significance of these features are set forth in the Amendment of August 13, 2003 and are repeated below for the Examiner's convenience. The examiner has failed to address in the final office action the arguments that are repeated below. It is respectfully requested that the examiner respond specifically to these arguments, since these issues are already before the examiner prior to the issuance of the final office action.

The reasons given by the examiner for the rejection of claims 15-17 and 19-21 (which are identical to those in the prior office action mailed March 13, 2003) fail to address and appear to have little to do with the specific limitations in these claims. The examiner is of the opinion that these claims are obvious in view of Kurumisawa, referring to Figure 34A and 710, 720, Li, Si. Such figure of Kurumisawa clearly fails to teach or suggest Claims 15-17 and 19-21. The examiner is of the opinion that *Kurumisawa* teaches these limitations because it teaches "a voltage source 700 connected to the row and column drivers." At the outset, it is noted that Figure 34A of *Kurumisawa* fails to show any row and column drivers separate from source 700, contrary to the examiner's opinion. As explained above, since the row and column electrodes are disconnected from

the voltage source 700 during the high impedance mode, the fact that voltage source 700 is present and perhaps somehow even connected to the missing "row and column drivers" is irrelevant, since whatever voltage is supplied by source 700 is also disconnected from the row and column electrodes. In any event, the teachings cited by the examiner in rejecting these claims, even if considered relevant, simply fail to teach anything even resembling the limitations in these claims.

Claims 15-22 are believed to be allowable since they depend from allowable Claim 14; they are further believed to be allowable because of the limitations added in these claims. Thus Claim 15 adds the limitation that the first voltage range is between a non-scanning voltage value and the scanning voltage value and the second voltage range changes with the non-scanning value. Claim 16 adds the limitation that the second power source comprises a pair of capacitors and the apparatus further comprises a switching circuit connecting the first power supply to the capacitors to cause the second voltage range to change about the non-scanning value. Claim 17 adds the limitation that the pair of capacitors are connected in a voltage divider configuration separating three nodes, wherein the switching circuit causes one of the nodes in between the pair to be at the non-scanning voltage of the first voltage range in at least one field addressing cycle. Claim 18 adds the feature that a switching circuit causes voltages at one of the two remaining nodes to be supplied to a column electrode during at least one field addressing cycle. Claim 19 adds a feature similar to a limitation in allowed Claim 1.

Claim 20 adds the limitation that the column electrodes are substantially disconnected from column drivers during the fraction of a portion of the addressing cycle when the capacitors are charged so that a desired image is displayed at pixels covered by the column electrodes that are substantially disconnected from the column drivers. As noted on page 12, lines 23-29 of the application, in one embodiment, when the column electrodes are so disconnected, the intrinsic capacitance of the liquid display itself performs as the holding capacitor until the capacitors are reconnected to them. This is different from Kurumisawa since, in claim 20, images are displayed so that a desired image is displayed at pixels covered by column electrodes that are so disconnected.

Claim 21 adds the feature that the first and second power sources supply only electrical potentials that are higher or lower than a referenced potential of the substrate.

Claim 22 contains the feature that the charge from the column electrode during one column addressing cycle is stored in a capacitor and is then re-used and applied to a column electrode in a subsequent column addressing cycle. This is described under the heading "Current Reuse" on pages 9 and 10 of the specification. None of these features is taught or suggested by Kurumisawa, Koshobu or any other art of record.

Claim 47 is likewise believed to be allowable since it depends from allowable Claim 14 and on account of the limitation added in this claim. As noted above, in the sections of *Kurumisawa* referred to by the examiner in the rejection (of claim 48; no valid reason is given for rejecting claim 47)), at least one or more of the switches are open during the high-impedance mode so that the data or scanning lines connected to such switches are simply not connected to any voltage source. Therefore, the sections relied on in the rejection in *Kurumisawa* also fail to teach or suggest the feature of Claim 47 where changes of the first and second voltage ranges of Claim 14 occur in a predetermined timing relationship to the addressing cycles. In *Koshobu,* all of the output voltages Vwp, Vhp, Ve, Vhn and Vwn of circuit 40 applied to the row (scanning) electrodes and the output voltages V1-V8 of circuit 50 applied to the column (signal) electrodes are generated at all times, so that any change or fluctuation in these voltages are unrelated to the timing of the addressing cycles. Hence, *Koshobu* also fails to remedy the deficiencies of *Kurumisawa* and, therefore, also fails to teach or suggest Claim 47.

Claim 48 covers a feature where at least one of the electrical potentials supplied to the row and column electrodes changes with a voltage supplied or caused to be supplied by one of the power sources and the change occurs in a predetermined timing relationship to the addressing cycles. In reference to Figure 2a of the present Application, this means that the circuits supplying electrical potentials to the row and column electrodes is such that at least one of the electrical potentials supplied to the row and column electrodes changes with the voltage supplied or caused to be supplied by one of the power sources and said change occurs in a predetermined timing relationship to the addressing cycles such as field 2xN and 2xN+1 illustrated in Figure 2a. In one embodiment, for example, the circuit may be a switching circuit connected to at least two power sources for generating electrical potentials to be applied to the row and column electrodes where the switching of the switching circuit occurs at a timing in a predetermined timing

relationship to the addressing cycles, it being understood that Claim 48 is not limited in scope to such embodiment. The sections relied on in the rejection in *Kurumisawa* also fail to teach or suggest the above feature of Claim 48. In *Koshobu,* all of the output voltages Vwp, Vhp, Ve, Vhn and Vwn of circuit 40 applied to the row (scanning) electrodes and the output voltages V1-V8 of circuit 50 applied to the column (signal) electrodes are generated at all times, so that any change or fluctuation in these voltages are unrelated to the timing of the addressing cycles. Hence, *Koshobu* also fails to remedy the deficiencies of *Kurumisawa* and, therefore, also fails to teach or suggest Claim 47.It is submitted that neither Kurumisawa nor *Koshobu*, either individually or in combination, teaches such feature. Claim 48 is, therefore, also believed to be allowable.

The examiner admits that *Kurumisawa* fails to teach two separate power sources, but is of the opinion that this missing teaching is supplied by *Koshobu.* However, there appears to be no reason or motivation to combine *Koshobu* and *Kurumisawa.* The reason given by the examiner for the combination (to provide a display capable of easily reducing flicker) simply does not apply to *Kurumisawa.* As noted above, *Kurumisawa.* is primarily interested in reducing power use, and in fact is turning off a portion or all of the display to reduce power consumption, and not to reduce flicker. There is therefore no reason or motivation to combine *Koshobu* and *Kurumisawa,* and the rejection of claim 48 also fails for this reason.

Claims 1-11, 13-22, 25-29, 31-39 and 41-48 are presently pending in the Application. Reconsideration of the rejections is respectfully requested and an early indication of the allowability of all the Claims is earnestly solicited.

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope address to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on June 21, 2004.

Franklin Dyer

Respectfully submitted,

James S. Hsue
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6/21/04
Date